FPGA IMPLEMENTATION OF A 64 POINT RADIX-2 SINGLE PATH DELAY FEEDBACK FFT ARCHITECTURE

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Abstract: Fast Fourier Transform (FFT) has huge area of applications. Orthogonal Frequency Division Multiplexing (OFDM) based wireless LAN uses 64 point FFT. In this paper, the complete design and FPGA implementation of a 64 point FFT processor using radix-2 Single-path Delay Feedback (SDF) architecture is presented. Very High Speed Integrated Circuits Hardware Description Language (VHDL) is used for the design and Xilinx ISE tools are used for the synthesis on Vertex 4 FPGA. Xpower Analyzer is used for power analysis.

Keywords: FFT, Wireless LAN, FPGA, Single-path Delay Feedback.

Introduction: Discrete Fourier Transform (DFT) is used for the spectral analysis of discrete signals. It is defined as shown in equation (1)

$$X(k) = \sum_{n=0}^{N-1} x(n) W_N^{kn}, \quad k = 0,1,2,3,\dots,N-1 \quad ---(1)$$

Where $x(n)$ is the discrete signal, $X(k)$ is the DFT of $x(n)$ and $W_N^{kn} = e^{-j\frac{2\pi nk}{N}}$ is called as the twiddle factor. The direct computation of equation (1) requires an order of N^2 complex operations whereas FFT greatly reduces the operations to an order of N(logN). FFT achieves this reduction by utilizing the periodicity and symmetry properties of the twiddle factor [1]. Cooley Tukey algorithms are proved to be the best suitable for VLSI implementations due to their simple and regular structure among various algorithms to compute FFT [2]. There are various architectures to implement the FFT algorithms in hardware such as memory based, pipelined and array architectures, etc. Pipelined architectures are preferred over the other architectures due to their pipelined nature for high throughput and capability of handling real time data [3]. This work mainly focused on FPGA implementation of the radix-2 Cooley Tukey algorithm using pipelined SDF architecture for a 64 point FFT computation which is used in OFDM based WLAN [4][5].

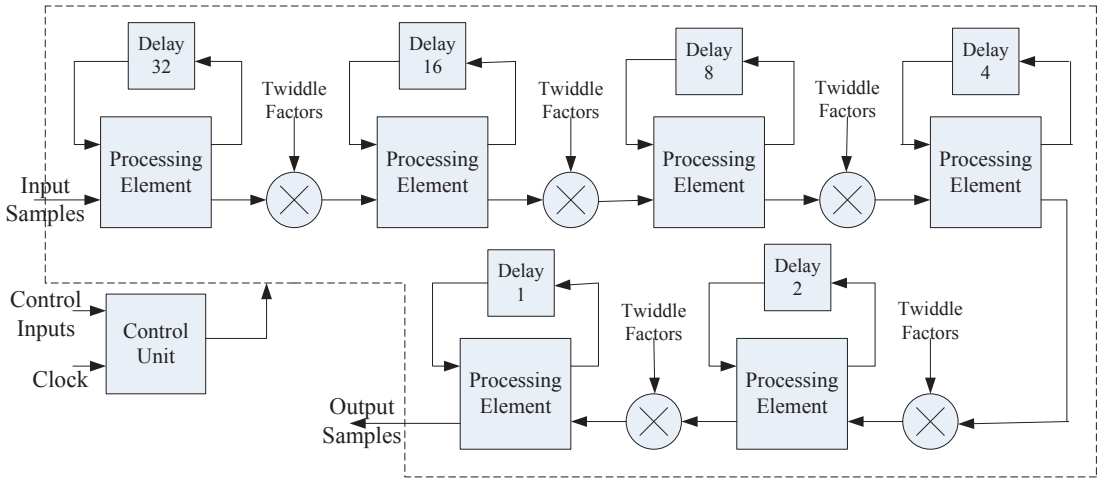

Fig.1. 64 point radix-2 SDF FFT architecture

64 point radix-2 SDF FFT processor architecture: Fig.1 shows the SDF architecture for a 64 point radix-2 FFT. It has a 6 stage pipeline that enables each Processing Element (PE) to

work in parallel. The input serial data invading into the processor are performed the butterfly operations between the right samples using proper delay. PE in all the 6 stages has the same hardware and selectively performs the radix-2 butterfly operation. Multiplier units are used to perform the twiddle factor multiplications where twiddle factors supplied to multiplier are gradually reduced from the first stage to the last by a factor 2. This is same as the number of delays in delay units at each stage as shown in Fig.1.

Design and FPGA Implementation of the Proposed Processor: The PE can be designed as shown in Fig.2 with de-multiplexers, multiplexers and a Butterfly Unit. Multiplexers and de-multiplexers are used to select whether or not the butterfly operation is performed. Butterfly Unit is a sample structure with two adders and two subtractors as shown in Fig.3 to carry out the addition and subtraction operations of both real and imaginary parts of the complex input data.

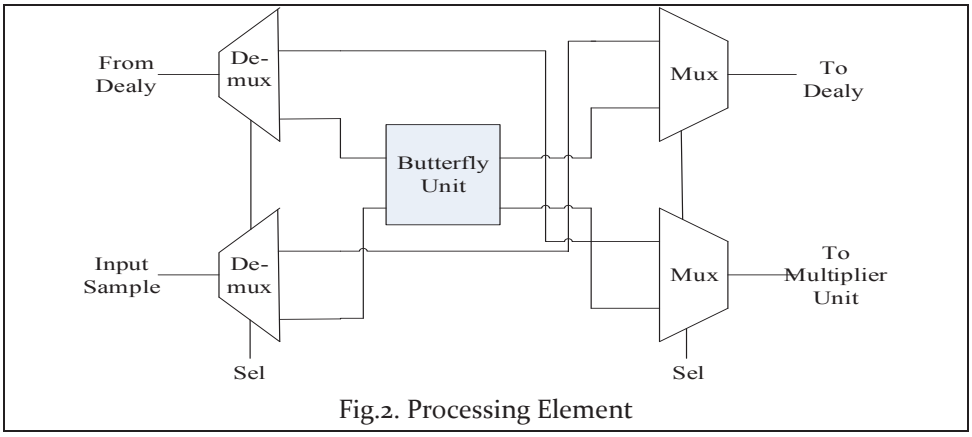

Fig.2. Processing Element

Fig.4 shows the Multiplier unit that selectively performs the complex multiplication between twiddle factors stored in ROM and the data samples after butterfly operation. The control unit supplies the select signals for both the processing element and multiplier unit. It takes clock signal and some control signals like reset and start as inputs to generate the select signals for all the stages.

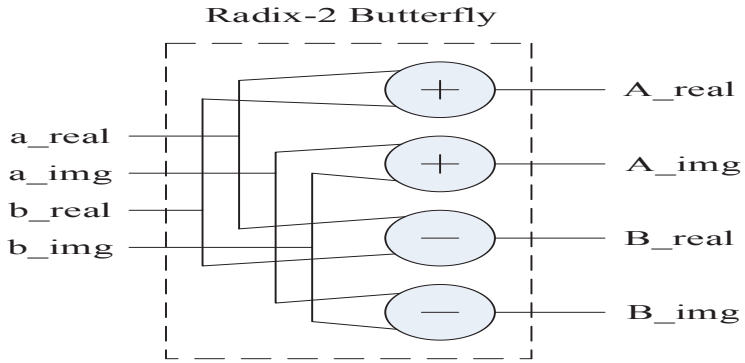

Fig.3. Butterfly Unit

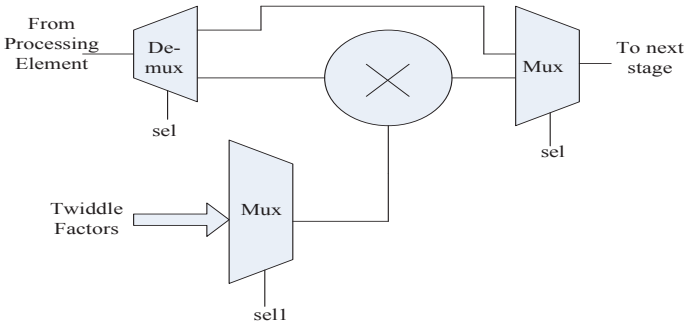

Fig.4. Multiplier Unit

VHDL code is written for all the modules and simulated using ISIM simulator. The post route simulation results are shown in Fig.5. For synthesis Vertex 4 FPGA and Xilinx synthesis tools are used. Fig.6 shows the RTL schematic of the proposed processor.

Results: The results obtained after synthesis and power analyses are depicted in the Table 1. The data length of the input samples and twiddle factors is taken as 16 bits. Simulation is run for a period of 2000 ns with data vectors to observe the dynamic power. The proposed design utilizes 1023 slices out of 5472, 1373 flip flops out of 10944 and 1520 LUTs out of 10944 available in the FPGA.

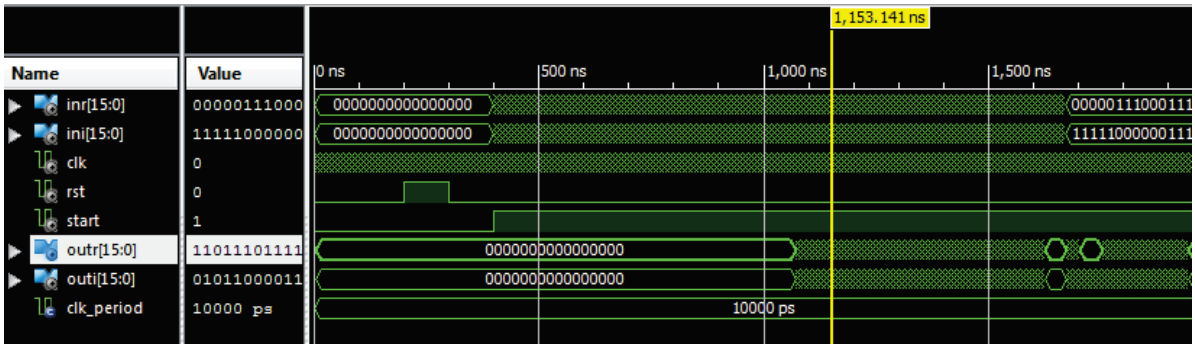

Fig.5. Post route simulation results

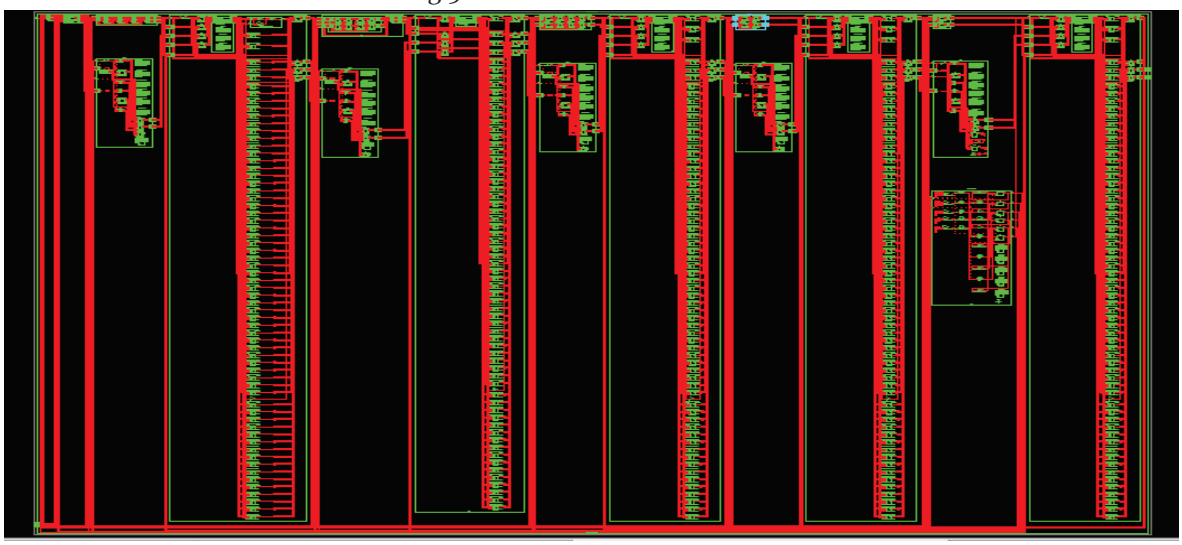

Fig.6. RTL schematic of the proposed design

Table 1. Results of synthesis and power analysis	
Percentage of slices used	18
Percentage of flip-flops used	12
Percentage of LUTs used	13
Maximum frequency (M Hz)	187.578
Static Power Consumption (mW)	170
Dynamic Power Consumption (mW)	186
Total Power Consumption (mW)	356

Conclusion: A radix-2 64 point pipelined SDF FFT processor is designed using VHDL and implemented on Vertex-4 FPGA. The parameters like resource utilization, maximum frequency of operation and power are observed and presented. This work can be extended to higher radix algorithms to analyze the power consumption and other parameters.

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